Tertiary Infotech Academy
Course Development | Training | Agentic AI Automation

Course Code: **M423**

Verilog Programming Training for FPGA

Funding Available: HRDF

COURSE INFORMATION

Sessions	Duration	Level	Assessment
2 days	15 hrs	Beginner	NA

VENUE

Kuala Lumpur: G-3A-02, Suite Pejabat Korporat, KL Gateway, No 2, Jalan kerinchi, Gerbang kernichi Lestari, 59200 Kuala Lumpur, Malaysia
Penang: Jalan Sungai Dua, 11700 Penang, Malaysia.

WHAT'S THIS COURSE ABOUT

Day 1

FPGA Design FLOW

Motivation

Topic 1 : Architecture of FPGA

Introduction to Programmable logic device (PLD)

Architecture

Structure of PLD

Topic 2 : Introduction to Verilog

Levels of Abstraction

Syntax & Semantics

Reserved Keywords

Topic 3: Verilog Ports

Ports declaration

Data types

Physical

Abstract

Constant

Topic 4: Operators

Arithmetic Operator

Bit...

COURSE FEE

Full Fee RM 2,000.00

CERTIFICATION

- **Certificate of Completion from Tertiary Courses** - Upon meeting at least 75% attendance and passing the assessment(s), participants will receive a Certificate of Completion from Tertiary Courses.

REGISTRATION

https://www.tertiarycourses.com.my/verilog-programming-training-for-fpga.html

SCAN TO REGISTER

SUPPORT

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